AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A microprocessor ~~built~~ on a semiconductor chip comprising:

a central processing unit adapted to execute instructions and generate address signals;

an external bus interface control circuit coupled to said central processing unit via an internal bus, adapted to control an external bus based on execution of instructions by said central processing unit, and being capable of activating one of a plurality of external device select signals, which is provided to an outside of said microprocessor corresponding to said address signals;

a clock generating circuit, coupled to said central processing unit, adapted to generate a plurality of clock signals including a first clock signal, a second clock signal and an internal clock signal;

a clock switching control circuit adapted to control an operation to switch a synchronous clock signal providing one of said first clock signal and said second clock signal to said external bus interface control circuit in accordance with said external device select signal;

a first clock terminal adapted to supply said first clock signal to a first external device which is to be coupled to said microprocessor; and

a second clock terminal adapted to supply said second clock signal to a second external device which is to be coupled to said microprocessor;

wherein said clock generating circuit provides said internal clock signal to said central processing unit,

wherein said second clock signal has a different frequency from said first clock signal, and

wherein said first and second clock signals are output from said microprocessor to said first and second external devices, respectively, in parallel.

2. (Previously Presented) A microprocessor comprising:

a central processing unit for executing instructions and generating at least one external access address; and

an external bus interface control circuit which controls an external bus based on execution of said instructions by said central processing unit,

wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to said external access address,

wherein said microprocessor includes a clock switching control circuit and a clock pulse generator,

wherein said clock switching control circuit controls an operation to switch a synchronous clock signal of said external bus interface control circuit to one of a first clock signal in accordance with activation of said first external device select signal and a second clock signal in accordance with activation of said second external device select signal,

wherein said clock pulse generator generates said first clock signal, said second clock signal and an internal clock signal,

wherein said first clock signal has a predetermined frequency different from that of said second clock signal,

wherein said clock pulse generator provides said internal clock signal to said central processing unit, and

wherein said microprocessor includes first and second external clock output terminals outputting said first and second clock signals, respectively, in parallel.

Claims 3-5 (Canceled).

6. (Previously Presented) The microprocessor according to claim 2,

wherein said clock switching control circuit requests said central processing unit to suspend execution of

instructions in response to activation of a selected external device select signal, and

wherein said clock switching control circuit is further capable of switching said synchronous clock signal, which is provided to said external bus interface control circuit, after an acknowledgment of the request to suspend instruction execution.

7. (Previously Presented) The microprocessor according to claim 6, wherein said clock switching control circuit is capable of switching said internal clock signal of said central processing unit in accordance with switching said synchronous clock signal of said external bus interface control circuit.

8-14. (Canceled)